REMARKS

The Examiner objected to the drawings, stating "because in Fig. 1 Clean GND 150 should be change to Clean GND 145. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application" and " The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: ground node network 285."

In response, Applicants have amended FIG. 1 to change Clean GRD 150 to Clean GND 145 without adding new matter. However, Applicant has examined FIG. 3 of sheet 3 and finds that the ground node element 285 appears on both the original drawing and in the "TIFF" file electronically filed with the application. Applicant has attached an additional copy of drawing sheet 3. The Examiner is directed to the right hand side of drawing sheet 3 where the numeral 285 appears next to the lower bracket.

The Examiner has stated "Claims 7, 9-15 and 22, 24-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Applicant gratefully acknowledge the Examiner's indication of allowable subject matter and has amended claims 9 and 24 to be in independent form and include all the limitations of the base claims and all intervening claims.

The Examiner rejected claims 1-6, 8, 16-21 and 23 under 35 U.S.C. §102(b) as being unpatentable over US Patent 5,428,299 to Koshikawa.

Applicant respectfully traverses the §102(b) rejections with the following arguments.

35 USC § 102

As to claims 1 and 16, the Examiner states that "Koshikawa et al discloses a voltage regulated power supply test circuit [see Fig. 5] comprising: a voltage regulator (built-in step down voltage generator 26) electrically connected to at least one regulated voltage node of a functional circuit (peripheral circuit 22) of an integrated circuit chip (semiconductor chip 21); and a circuit (monitoring circuit 25) capable of selectively connecting between one of said at least one regulated voltage nodes and ground with at least one load circuit (load transistors Qp16-17 and Qn18-19 or voltage divider 25b) adapted to put an emulated current load of said functional circuit (22) on said regulated voltage supply."

Applicant contends that claims 1 and 16, as amended, are not anticipated by Koshikawa because Koshikawa does not teach each and every feature of claims 1 and 16. As a first example Koshikawa does not teach "means for selectively and directly connecting at least one current load circuit between one of said at least one regulated voltage node and ground." Applicant respectfully points out that in Koshikawa teaches in FIG. 5, in col. 7, lines 46-53 and col. 8 lines 20-36 that a load circuit (which the Examiner cites as transistors Qp16-17 and Qn18-19 and voltage divider 25b) are not connected between a regulated voltage node of peripheral circuit 22 and ground as the Examiner asserts but rather are connected between an external voltage supply Vext on power supply pin Pext and ground.

Additionally, for claim 1, Koshikawa does not teach "in response to a control signal." Applicant points out, monitoring circuit 25 of Kohikawa is responsive to a change in voltage level of the external power supply Vext while in Applicants claim the "means for selectively and directly connecting" are responsive to "a control signal" which is a different and distinct element from Applicants "external power supply."

Additionally for claim 16, Koshikawa does not teach a "said at least one current load circuit adapted to put an emulated current load on said voltage regulated power supply, said emulated current load emulating a current load of said functional circuit on said voltage regulated power supply." Applicant points out that there is no teaching in Koshikawa that the load circuit (which the Examiner cites as transistors Qp16-17 and Qn18-19 and voltage divider 25b) are *emulating* any load generated by peripheral circuit 22. Further Applicants contend that is an impossibility for transistors Qp16-17 and Qn18-19 and voltage divider 25b to act as a load on the "regulated voltage power supply as the Examiner asserts. Applicant believes the Examiner understands that a load generated by peripheral circuit 22 would be applied to the output of voltage generator 26 labeled in Koshikawa FIG. 5. Applicant points out that Koshikawa teaches in FIG. 5, in col. 7, lines 46-53 and in col. 8 lines 20-36 that transistors Qp16-17 and Qn18-19 and voltage divider 25b are used as are used to generate signal Sdc which is used to select the voltage output level of voltage generator 26. Applicants further point out it is impossible for transistors Qp16-17 and Qn18-19 and voltage divider 25b to act as a load on the output of voltage generator 26 based on the teaching of Koshikawa in FIGs. 1 and 2 and in col. 1 line 47 though col. 3 line 3 which describe voltage generator 26 in detail and its response to the Sdc signal generated by Qp16-17 and Qn18-19 and voltage divider 25b.

Based on the preceding arguments, Applicant respectfully maintains that claims 1 and 16 are not unpatentable over Koshikawa and are in condition for allowance. Since claims 2-8 depend from claim 1 and claims 17-23 depend from claim 16, Applicant respectfully maintains that claims 2-8 and 17-23 are likewise in condition for allowance.

As to claims 4 and 19, the Examiner states that "Koshikawa et al discloses said load circuit (voltage divider 25b) comprises a gated resistive load (R5 and R6)." Applicant contends

that resistors R5 and R6 are not part of a load circuit as defined in Applicants claims 1 and 16 since voltage divider 25b generates a control signal selecting the voltage output level of voltage generator 26 making it is impossible for voltage divider 25b to act as a load on the output of voltage generator 26.

As to claims 5 and 20, the Examiner states that Koshikawa et al discloses said load circuit (load transistors Qp16-17 and Qn18-19) comprises a current mirror [see col. 7, lines 42-44]." Applicant contends that transistors Qp16-17 and Qn18-19 are not part of a load circuit as defined in Applicants claims 1 and 16 since transistors Qp16-17 and Qn18-19 generate a control signal selecting the voltage output level of voltage generator 26 making it is impossible for transistors Qp16-17 and Qn18-19 to act as a load on the output of voltage generator 26.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
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Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 1. This sheet, replaces the original sheet 1. In FIG. 1, clean GND element 150 had been changed to element 145.

Attachment: Replacement Sheet